2312-0866-2PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF :

KIMIHIRO MATSUSE ET AL. : EXAMINER: QUACH, T.

SERIAL NO. 09/530,588 : GROUP: 2814

FILED: MAY 5, 2000 :

FOR: WIRING STRUCTURE OF SEMICONDUCTOR DEVICE, ...

DECLARATION UNDER 37 C.F.R. §1.132

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

SIR:

We, Kimihiro Matsuse and Hayashi Otsuki, declare and state that:

1. We are citizens and residents of Japan, and the sole inventors of the present invention. We were employees of Tokyo Electron Limited, the assignee of the above-identified application, at the time of the invention.

2. Attached Figures 1-5 were submitted in the amendment filed on September 24, 2001 in response to the Official Action dated May 22, 2001.

3. Figure 1 shows the relationship between a value x of WN_x and the sheet resistance obtained after a rapid thermal anreal (RTA). Figure 2 shows the relationship between the values, y and z, of WSi_yN_z and the sheet resistance. Figures 1 and 2 depict data for samples whose alloy range is marginally greater than the claimed alloy ranges. The bar chart indicated by "Initial" shows data (sheet resistance) before the heat treatment. The other bar charts show data after the heat treatment.

4. The sheet resistance of conventional alloys is usually high after a heat treatment. However, the resistance values obtained with the claimed alloys of the present invention are low. This low resistance indicates that tungsten does not diffuse into the polysilicon layer during the RTA. If tungsten had diffused into the polysilicon layer, the formation of WSi would have generated voids between the tungsten and the polysilicon layer, resulting in a high sheet resistance.

5. If x, y, z of a tungsten nitride or a tungsten silicon nitride alloy exceed the values shown in Figures 1 and 2, a sheet resistance rapidly increases to several ohms, and often to several tens of ohms. Resistance values of several ohms to several tens of ohms are considered as high relative to the resistance values shown in the attached Figures 1 and 2. An alloy range of diffusion barriers which do not exhibit after anneal a high sheet resistance has been found for the first time by the declarants.

6. Figure 3 is a cross-sectional view of a layer whose x, y, z values fall within a range of tungsten silicon nitride of the present invention. As can be seen from Figure 3, the interface is remarkably planar.

7. Figure 4 is a cross-sectional view of a tungsten silicon nitride layer whose x, y, z values are outside the range of the present invention. Figure 4 shows that for alloy ranges outside the claimed range of the present invention, tungsten can diffuse into the polysilicon layer, creating a roughened non-planar interface. Furthermore, adhesiveness is damaged in the alloy shown in attached Figure 4 such that it becomes impossible to measure a resistance value for this alloy. Figure 5 shows a W depth profile obtained by secondary ion mass spectroscopy (SIMS) on a W/WN/poly-silicon structure of the present invention, after a RTA. Figure 5 shows that the concentration of W in the polysilicon layer is more than three orders

of magnitude lower than the concentration of W in the WN diffusion barrier following the RTA.

8. Tungsten nitrides and the tungsten silicon nitrides in the claimed ranges of the present invention produce adherent W diffusion barriers capable of preventing W diffusion during RTA, yielding planar interfaces and low sheet resistance electrical contacts.

9. We further declare that all statements made herein of own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: October 25, 2001

Kimihiro Matsuse
KIMIHIRO MATSUSE

Date: October 25, 2001

Hayashi Otsuki
HAYASHI OTSUKI

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